3D Chips: Stacked 2D Or Smarter Designs?

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Judging from the attention 3D chip manufacturing is getting, it looks as if it will soon become mainstream. Nearly every chip manufacturer is working on 3D, and every week, there is a 3D conference somewhere. But at the same time, the open questions and technological options surrounding 3D abound. Are we in for a 3D chip future? Or will 3D chips be limited to a few niche applications? And how far can we take 3D? Do we simply stack 2D designs, or can we design smarter, specific 3D architectures? Will we be able to manufacture those new 3D designs, technically and economically?

Notwithstanding these many questions surrounding the future of 3D chips, the first products have already hit the market. Flash memory cards, for examples, are made of stacked memory chips, drastically increasing the number of memory cells per package. This way, 3D chips are already part of the scaling story – the continuous drive for smaller, faster and cheaper ICs. Where 2D miniaturisation is faced with ever more complex challenges, it seems as though 3D can maintain Moore's momentum. And, on top of that, 3D offers a number of interesting new design possibilities.

Stacked 2D chips

3D IC manufacturing and research – as we know it today – comes in 3 flavours.

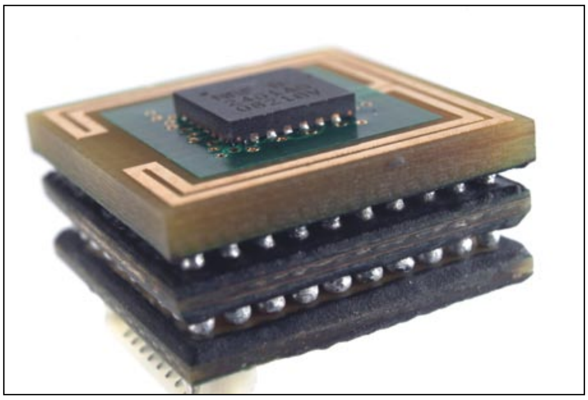


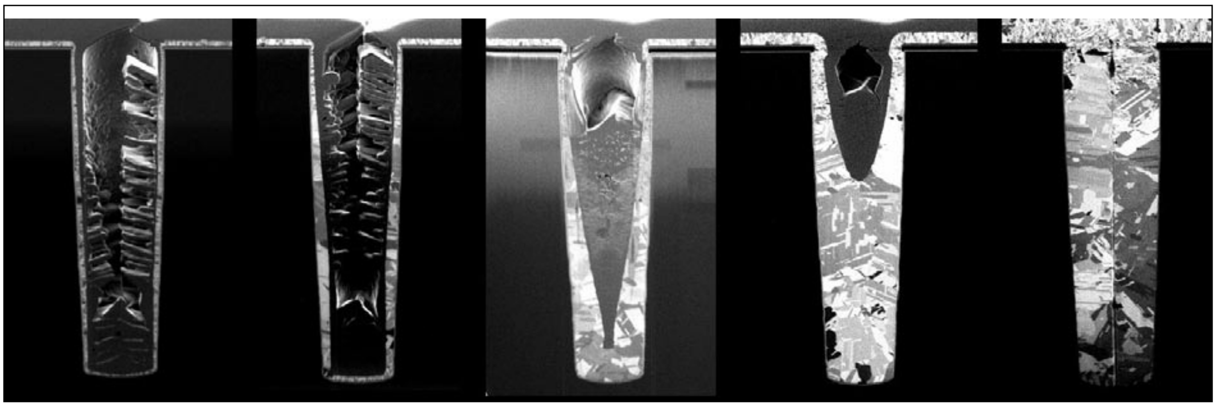
Figure 1 – Lead-free triple solder ball stack

Packaging a stack of standard 2D chips is a first possibility. This way of working does not change the chip design or the foundry processes; only the packaging process is involved. The chips are wire-bonded: the connections are made outside of the chips. An obvious example of a product available today is a memory package of, say, 16Gbyte, made of stacks of Flash memory chips. But it is also possible to stack a logical chip and one or more memory chips, or a sensor, a logical chip and a memory chip.

Through-silicon vias for direct contacts

Round, micro-sized holes etched in the silicon and filled with copper are the basis of the second technique. If the silicon wafer is then thinned until the copper nails stick out at the backside, we have chips with through-silicon contacts, or vias as they are also called. Next, the thinned wafer is placed on top of a second one, so that the copper nails on the backside of the thinned wafer contact the landing pads on top of the second wafer. This technique allows for direct contact points between the chips, making interconnect many orders of magnitude shorter and denser than those of wire-bonded packages. But this technique requires a specific chip design that distributes the components optimally over the 2 or more layers. And also the production process will change. The transistors, for example, have to be placed on the silicon such that there is

Figure 2 – Cross section of partially metallized through-Si vias; from left to right the plating duration increases



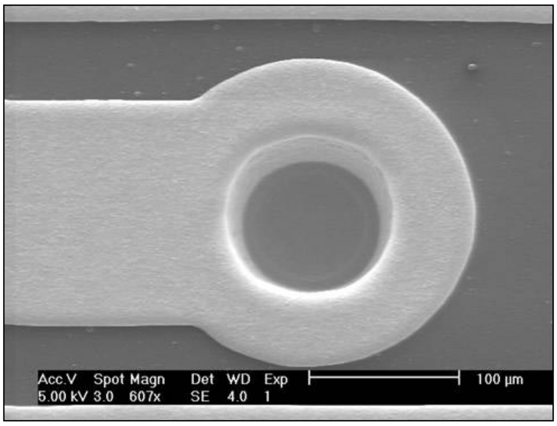


Figure 3 – Wafer-level packaging through-silicon via

room for the vias. And then the vias have to be etched and filled. Last, the chips have to be positioned over each other with extreme precision.

Over the next few years, research centres and chip manufacturers will perfect this technique. And following the introduction of the first 3D chips with through-silicon vias, there will again be a lot of opportunities for further scaling. We can go on making thinner chips, smaller vias, and better designs.

3D chips

Venturing into extreme 3D, we arrive at a foundry-only technique where we build the chips themselves in three dimensions. One idea is to grow extremely thin layers of silicon on a carrier, diffuse the transistors into that layer, add an interconnection layer on top, grow a new silicon layer, and so on. The interconnection layers will contact one another through nano-vias through the silicon layers. Because these vias will be so small, they can be made extremely dense, so that connections between individual transistors become possible. It would then be possible, for example, to manufacture a layer with p-transistors only, connected to a layer with n-transistors. It goes without saying that the design phase for this type of chips will be paramount. But also the production process will be totally different from what we know today.

Only time will tell if this technique will ever be viable. Today, it is still in the first stages of research. And we still don’t know how much real value it will bring, and if such chips can be produced technically and economically.

Why 3D chips

Opportunities and technological options aside, there is also the question of why we would build chips in three dimensions. There are different possibilities that reinforce each other. First there is the possibility to maintain Moore’s momentum for a considerable time to come. Already the first 3D applications, for example Flash memories, show the promise of denser, smaller, cheaper chip stacks. And we are just beginning to use 3D possibilities. In other words: a new scaling landscape is opening up.

Second, if we design specifically for 3D, we can realise solutions that are very hard to achieve in 2D. In the current generation of chips, we are forced to place memories, such as an L1 cache, next to logical circuits. This is because today’s fast processors can no longer efficiently work with off-chip memory alone. But it is expensive to manufacture logic and memory in one process. A 3D design could solve this dilemma, connecting a logical layer with a dedicated memory layer. By keeping interconnects extremely short, this could make an efficient design.

Thirdly, we can use 3D for heterogeneous integration, stacking dedicated layers with different technologies, such as logic, MEMS, RF, or bioactive substrates. This way, 3D designs could form autonomous embedded ICs used in clothing or healthcare applications.

Large Print Area Screen Printing Platform Unveiled

Leading screen printing and mass imaging specialist DEK is to unveil a large area version of its Europa print platform at APEX. Called the Europa Vi, the new machine offers substrate printing to 24” x 24” (610mm x 610mm) on demand to meet the diverse volume, mix and size requirements of modern production environments.Designed for integrated manufacturing and process optimisation, Europa Vi delivers extended flexible substrate image size range from 1.50” x 2.00” (38mm x 50mm) up to 24” x 24” (610mm x 610mm), a 30% increase over the standard Europa platform. The systems is also able to handle large board products up to 16.5lb (7.5kg) in weight and 0.236” (6mm) thick, and features heavy duty remote board stops. Europa Vi accommodates DEK’s latest suite of Instinctiv productivity tools. Instinctiv majors on ease-of-use and ensures simple operator transition from other platforms. Product size conversion to large boards is enabled by fully adjustable transport rails and a two-speed board transport control system with software time lag control. The platform is pre-configured with an upgraded understencil cleaner deploying a 4-stage head providing cleaning for a 24” (610mm) wide image using wet, vacuum and dry strokes. A vacuum filtration unit is also included.

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High Feeder Count, Large Board Size SMT Platform

Europlacer, a designer and manufacturer of comprehensive SMT placement systems for the global electronics industry, introduced the iineo SMT platform. The iineo platform features many improvements to the Europlacer machine range such as a higher feeder count, increased board size and increased maximum component height. The platform uses the company's proven core features – turret head, intelligent feeders, powerful software – while introducing new technologies with linear motors and digital cameras. iineo is widely configurable, allowing for numerous different possibilities: single or dual linear motor gantry including a rotary turret head with 8 or 12 pickups; 1 or 2 board positioning mechanisms; oversized board options; feeders front and back or front only.

The single-head iineo can handle maximum PCB sizes of 700 x 460 mm with options to handle up to 1610 x 600 mm. The double-head system can handle maximum PCB sizes of 500 x 460 mm with options to handle up to 700 x 600 mm. Both the single and dual-head iineo systems can handle minimum PCB sizes of 60 x 60 mm, board thickness of 0.5 to 4.5 mm, maximum weight of 3 kg and under board clearance of 25 mm. Additionally, both feature board edge clearance of 3 mm above/5 mm below, and left to right, fixed front rail transport criteria with a height of 950 mm (adjustable from 890 to 975 mm). Board location on both is full edge clamping with fiducial correction, and both systems feature a SMEMA interface. Depending on the configuration, maximum placement rate can be between 14,000 and 26,000 cph.

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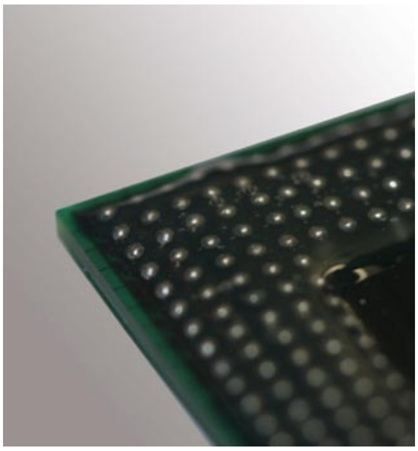
Epoxy Flux Technology Offers Cost-Effective Single Material Solution

Henkel has developed a new reflow cured encapsulant that combines flux functionality and underfill protection into a single material. The product, Hysol FF6000, is a reflow curable material that is formulated to provide flux for lead-free solder joint formation and, when cured, delivers protection against mechanical stress. Unlike traditional capillary underfill processes in which the device is mounted onto the printed circuit board, the assembly is reflowed and then the device is underfilled, Hysol FF6000 enables an in-line alternative that provides thorough device protection as well. With the epoxy flux process, bottom side spheres are dipped into Hysol FF6000 prior to component placement. The device is placed onto the printed circuit board or substrate and then travels through reflow. During the reflow process, the flux provides the action necessary for solder joint formation and the epoxy encapsulates each solder sphere, delivering added support and protection. This streamlined approach effectively eliminates the need for dispensing equipment and the time required for underfill application and cure. According to Henkel, Hysol FF6000 is particularly well-suited for today's Package-on-Package (PoP) device configurations and/or very large BGAs and CSPs where tradional underfill processes may be problematic. Second-level device attachment in emerging PoP applications is particularly challenging. Currently, many PoP device assemblers use tacky flux material for top level component attachment, which enables solder joint formation but does not resolve the issues pertaining to device support and protection.



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Range Of SN100C Soldering Materials Expanded

With its unique tin-copper-nickel-germanium alloy SN100C now firmly established as one of the global electronics industry's most popular lead-free wave soldering alloys, Nihon Superior announces that it is extending the range of material forms in which the alloy is available. Although developed initially to address the need for an economical wave solder, it has since been found that its properties also make SN100C an ideal choice for reflow and hand soldering as well as spheres for the attachment of area array packages.

The fluidity of SN100C, which is comparable to that of tin-lead, is one of the factors that contributes to excellent hole fill and minimal shorts in wave soldering. However, that property is also an advantage in hand soldering where, in combination with the right core flux (030), it makes possible the completion of more than 35 average joints per minute with a tip temperature of only 380°C. Nihon Superior is now offering the new eCore low-spatter lead-free flux-cored solder wire.

The 227°C melting point of SN100C was first thought to preclude its use in reflow soldering but when it was noted that tin-silver-copper alloys (such as SAC305 with a melting point of 217-218°C) are typically reflowed with a peak temperature around 245°C, it was realised that SN100C could be a drop-in replacement. Its high fluidity and excellent wetting properties mean that SN100C can be reflowed successfully at a lower superheat above liquidus than SAC alloys. Nihon Superior now offers two types of SN100C solder paste – no-clean ePaste for general reflow purposes and ePaste, a special low voiding paste for critical applications such as die attach in which heat transfer though the joint must be maximised.

Advantages of the tin-copper system include its ruggedness in impact loading and the nickel addition provides inhibition of the intermetallic growth that can increase the susceptibility of joints to failure in shock loading, e.g. when a mobile phone is dropped. These properties are prompting the industry to evaluate SN100C in flip chip and area array packages, and Nihon Superior is supporting this new application by making a range of eBalls available.

While a wide range of fluxes can used successfully in wave soldering with SN100C, Nihon Superior also is now offering eFlux, a new flux that has been specially formulated for optimum results.

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Modular Fluid Dispense System For Screen Printers

Ovation Products announces the introduction of its new Stinger fluid dispense system. According to Ovation, the company's patent pending dispense module will expand the capabilities of conventional screen printers by enabling the user to dispense SMT adhesive or solder paste on a PCB, immediately following the screen print operation while it is still in alignment from the screen print.

The small and lightweight dispense module is coupled to the printer's vision system by an electro-pneumatic interface that allows the entire module to be removed and reinstalled on the printer in seconds for ease of maintenance and material changeover. Once the PCB is screen printed (as normal), it is separated from the stencil and lowered back to "vision height" at which time the camera/Stinger will accurately dispense adhesive or paste (from industry standard cartridges) on a virtually unlimited number of user-defined sites while dynamically adjusting the dispense tip height, in case of board warpage, with its laser compensating servo-controlled Z-axis.

The system is field retrofit capable and eliminates the need for the added floor space, cost and maintenance associated with a dedicated inline dispenser.

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